#6/5-16-03
V. Jones

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Takaki YOSHIDA et al.

Serial No.: 09/697,305 Group Art Unit: 2133

Filed: October 27, 2000 Examiner: Joseph D. Torres

For: FAULT DETECTING METHOD AND LAYOUT METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Office Action mailed April 21, 2003, applicants hereby provisionally elect, with traverse, to prosecute the claims of Group I (claims 1-22) in this application.

However, applicants traverse the restriction requirement since the subject matter of all of claims 1-52 is sufficiently related that a thorough and complete search for the subject matter of the elected claims would necessarily encompass a thorough and complete search for the subject matter of the non-elected claims. Search and examination of the entire application could be made without

serious burden. See MPEP §803 which clearly states that "[i]f the search and examination of an entire application can be made without serious burden, the Examiner must examine it on the merits." This policy should apply in the present application to avoid unnecessary delay and expense to applicants and duplicative examination by the Patent Office.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

May 14, 2003
Date

Charles A. Wendel
Registration No. 24,453

CAW/mhs

Attorney Docket No.: YMOR:186

PARKHURST & WENDEL, L.L.P.
1421 Prince Street, Suite 210
Alexandria, Virginia 22314-2805
Telephone: (703) 739-0220